AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

AMENDMENTS TO THE CLAIMS:

1. (Currently Amended) A method of processing frames of data comprised of frameword bytes and a payload, comprising:

receiving data for a first frame;

storing the data for the first frame in N, N $\geq$2, registers;

identifying a start of the first frame of data and a phase of the first frame concurrently based on the frameword bytes, wherein the phase of the first frame is identified based on a location of the start of the first frame in at least one of the N registers; and

aligning data in a second frame of data, based on the phase of the first frame, to make a start of the second frame coincide with a start of a byte boundary.

2. (Previously Presented) The method of claim 1, wherein the frameword bytes identify the start of the first frame.

3. (Cancelled).

4. (Previously Presented) The method of claim 1, further comprising:

locating the start of the first frame in the N registers.

5. (Previously Presented) The method of claim 4, wherein locating the start of the first frame comprises:

comparing data for the first frame in the N registers to predetermined values for the frameword bytes.

6. (Previously Presented) The method of claim 1, wherein identifying the phase of the first frame comprises determining a location, in one of the N registers, of a first bit of data for a first frameword byte.

7. (Previously Presented) The method of claim 1, wherein the location of the start of the first frame in the N registers is determined based on whether a value stored in one of the N registers corresponds to a set of predefined values.

8. (Previously Presented) The method of claim 6, wherein aligning the data comprises shifting the first bit of data so that a first bit of data in the second frame is at a start of one of the N registers.

9. (Previously Presented) The method of claim 1, further comprising:

dividing the data for the first and second frames into blocks;

wherein the start of the first frame and the phase of the first frame are identified in one of the blocks and aligning is performed on the second frame.

10. (Previously Presented) The method of claim 1, further comprising:

identifying a predetermined number of frames following identifying the start of the first frame and the phase of the first frame;

wherein aligning is performed on the second frame after identifying the predetermined number of frames.

11. (Previously Presented) The method of claim 1, wherein the start of the byte boundary comprises a start of a word boundary.

12. (Currently Amended) An apparatus for processing frames of data comprised of frameword bytes and a payload, comprising:

a detector which identifies a start of a first frame of data and a phase of the first frame concurrently based on the frameword bytes, the detector comprising N, N $\geq$2, registers that receive and store the data for the first frame, the detector identifying the phase of the first frame based on a location of the start of the first frame in at least one of the N registers; and

a word rotator which aligns data in a second frame of data, based on the phase of the first frame, to make a start of the second frame coincide with a start of a byte boundary.

13. (Original) The apparatus of claim 12, wherein the frameword bytes identify the start of the first frame.

14. (Cancelled)

15. (Previously Presented) The apparatus of claim 12, wherein the detector locates the start of the first frame in the N registers.

16. (Original) The apparatus of claim 15, wherein the detector locates the start of the first frame by comparing data for the first frame in the N registers to predetermined values for the frameword bytes.

17. (Previously Presented) The apparatus of claim 12, wherein the detector identifies the phase of the first frame by determining a location, in one of the N registers, of a first bit of data for a first frameword byte.

18. (Previously Presented) The apparatus of claim 12, wherein the detector determines the location of the start of the first frame in the N registers based on whether a value stored in one of the N registers corresponds to a set of predefined values.

19. (Original) The apparatus of claim 17, wherein the word rotator aligns the data by shifting the first bit of data so that a first bit of data in the second frame is at a start of one of the N registers.

20. (Original) The apparatus of claim 12, further comprising:

circuitry which divides the data for the first and second frames into blocks;

wherein the detector identifies the start of the first frame and the phase of the first frame in one of the blocks and the word rotator performs aligning on the second frame.

21. (Original) The apparatus of claim 12, further comprising:

a state machine which identifies a predetermined number of frames following identifying the start of the first frame and the phase of the first frame;

wherein the word rotator performs aligning on the second frame after the state machine identifies the predetermined number of frames.

22. (Original) The apparatus of claim 12, wherein the start of the byte boundary comprises a start of a word boundary.

23. (Currently Amended) An article comprising a machine-readable medium that stores executable instructions to process frames of data comprised of frameword bytes and a payload, the instructions causing a machine to:

receive data for a first frame;

store the data for the first frame in N, N ≥2, registers;

identify a start of a first frame of data and a phase of the first frame concurrently based on the frameword bytes, wherein the phase of the first frame is identified based on a location of the start of the first frame in at least one of the N registers; and

align data in a second frame of data, based on the phase of the first frame, to make a start of the second frame coincide with a start of a byte boundary.

24. (Original) The article of claim 23, wherein the frameword bytes identify the start of the first frame.

25. (Cancelled)

26. (Previously Presented) The article of claim 23, further comprising instructions that cause the machine to:

locate the start of the first frame in the N registers.

27. (Original) The article of claim 26, wherein locating the start of the first frame comprises:

comparing data for the first frame in the N registers to predetermined values for the frameword bytes.

28. (Previously Presented) The article of claim 23, wherein identifying the phase of the first frame comprises determining a location, in one of the N registers, of a first bit of data for a first frameword byte.

29. (Previously Presented) The article of claim 23, wherein the location of the start of the first frame in the N registers is determined based on whether a value stored in one of the N registers corresponds to a set of predefined values.

30. (Original) The article of claim 28, wherein aligning the data comprises shifting the first bit of data so that a first bit of data in the second frame is at a start of one of the N registers.

31. (Previously Presented) The article of claim 23, further comprising instructions that cause the machine to:

divide the data for the first and second frames into blocks;

wherein the start of the first frame and the phase of the first frame are identified in one of the blocks and aligning is performed on the second frame.

32. (Original) The article of claim 23, further comprising instructions that cause the machine to:

identify a predetermined number of frames following identifying the start of the first frame and the phase of the first frame;

wherein aligning is performed on the second frame after identifying the predetermined number of frames.

33. (Currently Amended) A method of processing frames of data, comprising

receiving data for a first frame;

dividing the data for the first frame into blocks that are stored in registers;

using multiple comparators to analyze the blocks, each comparator analyzing at least two blocks that are non-consecutive in the first frame to determine a phase of the at least two blocks, where the phase corresponds to a location of the first frame in at least one register;

identifying a start of the first frame and a phase of the first frame based on the phases of the blocks determined by the multiple comparators; and

aligning data in a second frame of data, based on the phase of the first frame, to make a start of the second frame coincide with a start of a byte boundary.

34. (Previously Presented) The method of claim 33 wherein using multiple comparators to analyze the blocks comprises using multiple comparators to analyze the blocks in parallel.

35. (Previously Presented) The method of claim 33 wherein receiving data for a first frame comprises receiving data for the first frame through an N-byte parallel data path, N being equal to the number of blocks, each block processing an 8-bit portion of the N-byte data path.

36. (Previously Presented) The method of claim 33 wherein the frames of data comply with at least one of Synchronous Optical Networking and Synchronous Digital Hierarchy standards.

37. (Currently Amended) An apparatus for processing frames of data, comprising:

groups of registers to store blocks of a first frame, each group of registers for storing blocks that are non-consecutive in the first frame;

a plurality of comparators to analyze the blocks of the first frame, each comparator for determining a phase of the blocks stored in one group of registers, where the phase corresponds to a location of the first frame in at least one register;

a detector to identify a start of the first frame and a phase of the first frame based on the phases of blocks determined by the plurality of comparators; and

a word rotator to align data in a second frame of data based on the phase of the first frame to make a start of the second frame coincide with a start of a byte boundary and a word boundary.

38. (Previously Presented) The apparatus of claim 37 wherein the plurality of comparators operate in parallel.

39. (Previously Presented) The apparatus of claim 37 wherein each block processes 8 consecutive bits of a parallel data path, each word is equal to N bytes, and the plurality of comparators comprise N comparators.

40. (Previously Presented) The apparatus of claim 37 wherein the frames of data comply with at least one of Synchronous Optical Networking and Synchronous Digital Hierarchy standards.